An article in the AT & T technical journal (March/April 1986, Vol. 65, pp.- 39-50) describes the applications of two-level factorial design to integrated circuit mfg. A basic processing step is to grow an epitaxial layer on polished silicon wafers. The wafers mounted on a susceptor are positioned inside the bell jar, and chemical vapors are introduced. The susceptor is rotated, and heat is applied until the epitaxial layer is thick enough. An experiment was run using two factors; arsenic flow rate (A) and deposition time (B). Four replicates were run, and the epitaxial layer thickness was measured (µm). The data is shown in the following table;

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Factors | | Replicates | | | | Factors | Factor Levels | |
| A | B | R-I | R-II | R-III | R-IV | Low(-) | High (+) |
| - | - | 14.037 | 16.165 | 13.972 | 13.907 | A | 55 % | 59 % |
| + | - | 13.880 | 13.860 | 14.032 | 13.914 |
| - | + | 14.821 | 14.757 | 14.843 | 14.878 | B | Short  (10 Min) | Long  ( 15 Min) |
| + | + | 14.888 | 14.921 | 14.415 | 14.932 |

1. Estimate the factor effects.
2. Conduct an ANVA, which factors are important?
3. Write down a regression equation that could be used to predict epitaxial layer thickness over the region of arsenic flow rate and deposition time used in the experiment.
4. Analyze the residuals. Are there any residuals that cause of concern?